In The Claims

Amend claims 1, 4, and 6-8 as follows.

1. (amended) A method for making a nonvolatile, floating-gate memory with logic transistors in a face of a semiconductor body having a first conductivity type, comprising the steps of:

forming first and second opposite-conductivity-type diffusion regions [having a first depth] at a first time in said semiconductor body, said first and second opposite-conductivity-type diffusion regions doped to have primarily a second conductivity-type opposite said first conductivity-type;

forming first and second same-conductivity-type diffusion regions [having a second depth] at a second time in said semiconductor body, said first same-conductivity-type diffusion region encased in said first opposite-conductivity-type diffusion region, said second same-conductivity-type diffusion region separate from said first and second opposite-conductivity-type diffusion regions, said first and second same-conductivity-type diffusion regions doped to have primarily said first conductivity-type;

forming at least one floating-gate memory cell in and on said first same-conductivity-type diffusion region;

forming at least one high-voltage logic transistor in said second opposite-conductivity-type diffusion region; and

forming at least one low-voltage logic transistor in said second same-conductivity-type diffusion region.

4. (amended) The method according to claim 1, wherein Fowler-Nordheim [tunnelling] tunneling is used to program said floating [gates of memory cells] gate of said at least one memory cell.

6. (amended) The method according to claim 1, further including formation of field oxide regions on the surface of said semiconductor [substrate] body, said field oxide regions formed over the edges of said diffusion regions.

7. (amended) The method according to claim 1, further including formation of field oxide regions on the surface of said semiconductor [substrate] body, said field oxide regions formed over the edges of said diffusion regions and formed within said diffusion regions surrounding at least one connection point.

8. (amended) The method according to claim 1, further including formation of field oxide regions on the surface of said semiconductor [substrate] body, said field oxide regions formed to surround connection points to said diffusion regions, said first opposite-conductivity-type diffusion region and said first same-conductivity-type diffusion regions having multiple connection points at the periphery of said diffusion regions.

Add new claims 11-65 as follows.

11. The method according to claim 1, wherein said first and second opposite-conductivity-type diffusion regions have approximately a same depth.

12. The method according to claim 1, wherein said first and second same-conductivity-type diffusion regions have approximately a same depth.

13. The method according to claim 1, wherein said at least one high-voltage logic transistor is a P-channel transistor, and wherein said at least one low-voltage logic transistor is an N-channel transistor.

14. The method according to claim 1, comprising the step of applying a supply voltage having a first voltage with respect to ground to said at least one low-voltage logic transistor, said first voltage having a first magnitude.

15. The method according to claim 14, comprising the step of applying a high voltage having a second magnitude greater than said first magnitude to said at least one high-voltage logic transistor.

16. The method according to claim 14, comprising the step of applying a high voltage having a second magnitude greater than said first magnitude to a control gate of said at least one floating-gate memory cell during a write mode.

17. The method according to claim 14, comprising the step of applying a voltage having polarity opposite said first voltage to a control gate of said at least one floating-gate memory cell during an erase mode.

18. The method according to claim 1, wherein said at least one floating-gate memory cell comprises a drain terminal and a source terminal, and wherein said source terminal is floating during an erase mode.

19. The method according to claim 1, wherein said at least one floating-gate memory cell comprises a drain terminal and a source terminal, and wherein said source terminal is coupled to receive a high voltage during an erase mode.

20. The method according to claim 1, comprising the step of applying a ground voltage to said first opposite conductivity type diffusion region and to said first same conductivity type diffusion region during a write mode.

21. The method according to claim 1, wherein said at least one floating-gate memory cell comprises selected and unselected floating-gate memory cells, each floating-gate memory cell having a respective drain terminal and source terminal, and wherein a source terminal of said selected floating-gate memory cell is coupled to receive a ground voltage, and a source terminal of said unselected floating-gate memory cell is coupled to receive a voltage different from said ground voltage during a write mode.

22. The method according to claim 1, wherein said at least one floating-gate memory cell comprises plural arrays of floating-gate memory cells, each array of floating-gate memory cells comprising a sector of said nonvolatile, floating-gate memory, wherein each said sector includes a respective first opposite-conductivity-type diffusion region and a respective first same-conductivity-type diffusion region, said diffusion regions being separate from diffusion regions of other sectors.

23. The method according to claim 22, wherein each said respective first same-conductivity-type diffusion region includes a respective diffusion contact having said first conductivity type.

24. A method for making a memory with logic transistors in a face of a semiconductor body having a first conductivity type, comprising the steps of:

simultaneously forming first and second diffusion regions having a second conductivity type in said semiconductor body, said second conductivity type being opposite said first conductivity type;

simultaneously forming third and fourth diffusion regions having said first conductivity

type in said semiconductor body, said third diffusion region isolated from said semiconductor body by said first diffusion region, said fourth diffusion region separate from said first and second diffusion regions;

forming at least one memory cell in and on said third diffusion region;

forming at least one logic transistor having a channel in said second diffusion region; and

forming at least another logic transistor having a channel in said fourth diffusion region.

25. The method according to claim 24, wherein said semiconductor body is silicon of P conductivity-type, said first and second diffusion regions are N conductivity-type and said third and fourth diffusion regions are P conductivity-type.

26. The method according to claim 24, wherein said first and third diffusion regions are coupled to receive a positive voltage with respect to said semiconductor body during erasure of said memory cell.

27. The method according to claim 24, wherein Fowler-Nordheim tunneling is used to program said at least one memory cell.

28. The method according to claim 24, wherein Fowler-Nordheim tunneling is used to erase said at least one memory cell.

29. The method according to claim 24, wherein said memory cell is part of a nonvolatile, floating-gate memory array having single-dopant sources and drains.

30. The method according to claim 24, comprising the step of forming field oxide regions on the surface of said semiconductor body, said field oxide regions formed over the edges of said

diffusion regions.

31. The method according to claim 24, comprising the steps of:

forming at least one connection point within at least one of said first and third diffusion regions; and

forming field oxide regions within said at least one of said first and third diffusion regions surrounding said at least one connection point.

32. The method according to claim 31, wherein said at least one connection point comprises multiple connection points.

33. The method according to claim 31, wherein said at least one connection point comprises a diffused contact having a same conductivity type as said at least one of said first and third diffusion regions.

34. The method according to claim 32, wherein said diffused contact is formed by doped polysilicon.

35. The method according to claim 24, wherein said at least one logic transistor having a channel in said second diffusion region is a high voltage transistor arranged to receive a voltage having a greater magnitude than said at least another logic transistor having a channel in said fourth diffusion region.

36. The method according to claim 24, comprising the step of applying a low voltage having a first magnitude to said at least another transistor.

37. The method according to claim 36, comprising the step of applying a high voltage having a second magnitude greater than said first magnitude to a control gate of said at least one memory cell during a write mode.

38. The method according to claim 36, comprising the step of applying a voltage having polarity opposite said low voltage to a control gate of said at least one memory cell during an erase mode.

39. The method according to claim 24, wherein said at least one memory cell comprises a drain terminal and a source terminal, and wherein said source terminal is floating during an erase mode.

40. The method according to claim 24, wherein said at least one memory cell comprises a drain terminal and a source terminal, and wherein said source terminal is coupled to receive said high voltage during an erase mode.

41. The method according to claim 24, comprising the step of applying a ground voltage to said first and third diffusion regions during a write mode.

42. The method according to claim 24, wherein said at least one memory cell comprises selected and unselected memory cells, each memory cell having a respective drain terminal and source terminal, and wherein a source terminal of said selected memory cell is coupled to receive a ground voltage, and a source terminal of said unselected memory cell is coupled to receive a voltage different from said ground voltage during a write mode.

43. The method according to claim 24, wherein said at least one memory cell comprises plural arrays of memory cells, each array of memory cells comprising a sector of said memory, wherein each said sector includes a respective first and third diffusion region being separate from first and third diffusion regions of other sectors.

44. The method according to claim 24, wherein each said third diffusion region includes a respective diffusion contact having said first conductivity type.

45. A method for making a memory with logic transistors in a face of a semiconductor body having a first conductivity type, comprising the steps of:

forming first and second diffusion regions having a first concentration at a first depth and having a second conductivity type in said semiconductor body, said second conductivity type being opposite said first conductivity type;

forming third and fourth diffusion regions having a second concentration at a second depth and having said first conductivity type in said semiconductor body, said third diffusion region isolated from said semiconductor body by said first diffusion region, said fourth diffusion region separate from said first and second diffusion regions;

forming at least one memory cell in and on said third diffusion region;

forming at least one logic transistor having a channel in said second diffusion region; and

forming at least another logic transistor having a channel in said fourth diffusion region.

46. The method according to claim 45, wherein said semiconductor body is silicon of P conductivity-type, said first and second diffusion regions are N conductivity-type and said third and fourth diffusion regions are P conductivity-type.

47. The method according to claim 45, wherein said first and third diffusion regions are coupled to receive a positive voltage with respect to said semiconductor body during erasure of said memory cell.

48. The method according to claim 45, wherein Fowler-Nordheim tunneling is used to

program said at least one memory cell.

49. The method according to claim 45, wherein Fowler-Nordheim tunneling is used to erase said at least one memory cell.

50. The method according to claim 45, wherein said memory cell is part of a nonvolatile, floating-gate memory array having single-dopant sources and drains.

51. The method according to claim 45, comprising the step of forming field oxide regions on the surface of said semiconductor body, said field oxide regions formed over the edges of said diffusion regions.

52. The method according to claim 45, comprising the steps of:

forming at least one connection point within at least one of said first and third diffusion regions; and

forming field oxide regions within said at least one of said first and third diffusion regions surrounding said at least one connection point.

53. The method according to claim 52, wherein said at least one connection point comprises multiple connection points.

54. The method according to claim 52, wherein said at least one connection point comprises a diffused contact having a same conductivity type as said at least one of said first and third diffusion regions.

55. The method according to claim 53, wherein said diffused contact is formed by doped polysilicon.

56. The method according to claim 45, wherein said at least one logic transistor having a channel in said second diffusion region is a high voltage transistor arranged to receive a voltage having a greater magnitude than said at least another logic transistor having a channel in said fourth diffusion region.

57. The method according to claim 45, comprising the step of applying a low voltage having a first magnitude to said at least another transistor.

58. The method according to claim 57, comprising the step of applying a high voltage having a second magnitude greater than said first magnitude to a control gate of said at least one memory cell during a write mode.

59. The method according to claim 57, comprising the step of applying a voltage having polarity opposite said low voltage to a control gate of said at least one memory cell during an erase mode.

60. The method according to claim 45, wherein said at least one memory cell comprises a drain terminal and a source terminal, and wherein said source terminal is floating during an erase mode.

61. The method according to claim 45, wherein said at least one memory cell comprises a drain terminal and a source terminal, and wherein said source terminal is coupled to receive said high voltage during an erase mode.

62. The method according to claim 45, comprising the step of applying a ground voltage to said first and third diffusion regions during a write mode.

63. The method according to claim 45, wherein said at least one memory cell comprises selected and unselected memory cells, each memory cell having a respective drain terminal and

source terminal, and wherein a source terminal of said selected memory cell is coupled to receive a ground voltage, and a source terminal of said unselected memory cell is coupled to receive a voltage different from said ground voltage during a write mode.

64. The method according to claim 45, wherein said at least one memory cell comprises plural arrays of memory cells, each array of memory cells comprising a sector of said memory, wherein each said sector includes a respective first and third diffusion region being separate from first and third diffusion regions of other sectors.

65. The method according to claim 45, wherein each said third diffusion region includes a respective diffusion contact having said first conductivity type.